DOE F 1325.8e Electronic Form Approved by Forms Mgmt. 04/19/2006
(08-89)

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United States Government **Department of Energy**

Bonneville Power Administration

memorandum

DATE: January 20, 2016

REPLY TO ATTN OF: TPP/OPP-3

SUBJECT: Pacific HVDC Intertie AC-Voltage Dependent Current Order Limiter

TO: Melvin Rodrigues – TPP/OPP3
Margaret Albright – TOT/DITT2
Richard Ellison – TOD/DITT1
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1. Summary and Objectives

Folloiwng August 10 1996 system outage, BPA implemented AC Voltage-Dependent Current Order Limiter (AC-VDCOL) at the Pacific HVDC Intertie (PDCI). PDCI operates in constant power mode. It was determined based on the event analysis and system studies, that reducing PDCI power during low voltage power swings is benefitial for transient stability and oscillation damping. BPA Transmission Planning reviewed the need and concluded that AC-VDCOL is still very beneficial for system stability with new PDCI upgrades. AC-VDCOL will be implemented in new PDCI controls.

The objective of these tests is to verify AC-VDCOL dynamic performance. The tests will involve operation of the Chief Joseph braking resistor.

2. Test Dates

March 22, 2016 starting at 10:00 AM.
Alternative dates are March 23, March 29 or March 30, 2016.

3. Operating Conditions Required For Tests

Operating Conditions for Chief Joseph brake insertion tests

- Power system operation is normal, the system is within System Operating Limits
- BPA Oscillation Detection Application shows no oscillations, all PMUs and all boxes on the display are "green"-lit
- If BC-Alberta tie is in service, North-South Mode A is above 9%
- If BC-Alberta tie is out of service, North-South Mode B is above 5%
- Chief Joseph 500/230-kV transformer is in service
- Keeler 230-kV Static Var Compensator is in service
- Keeler 500/230-kV transformer is in service
- PDCI power is above 2,900 MW
- Big Eddy and Celilo 500-kV voltages are above 535-kV
- At least one Big Eddy 500/230-kV transformer is in service

4. Test Precautions and Termination Procedure

If at any time the Test Observers, security coordinators or system operators identify conditions under which the tests should not continue then the Test Director will suspend the test sequence until those conditions are no longer present and the Test Coordinator will have Dispatch send out a WECC Net message.

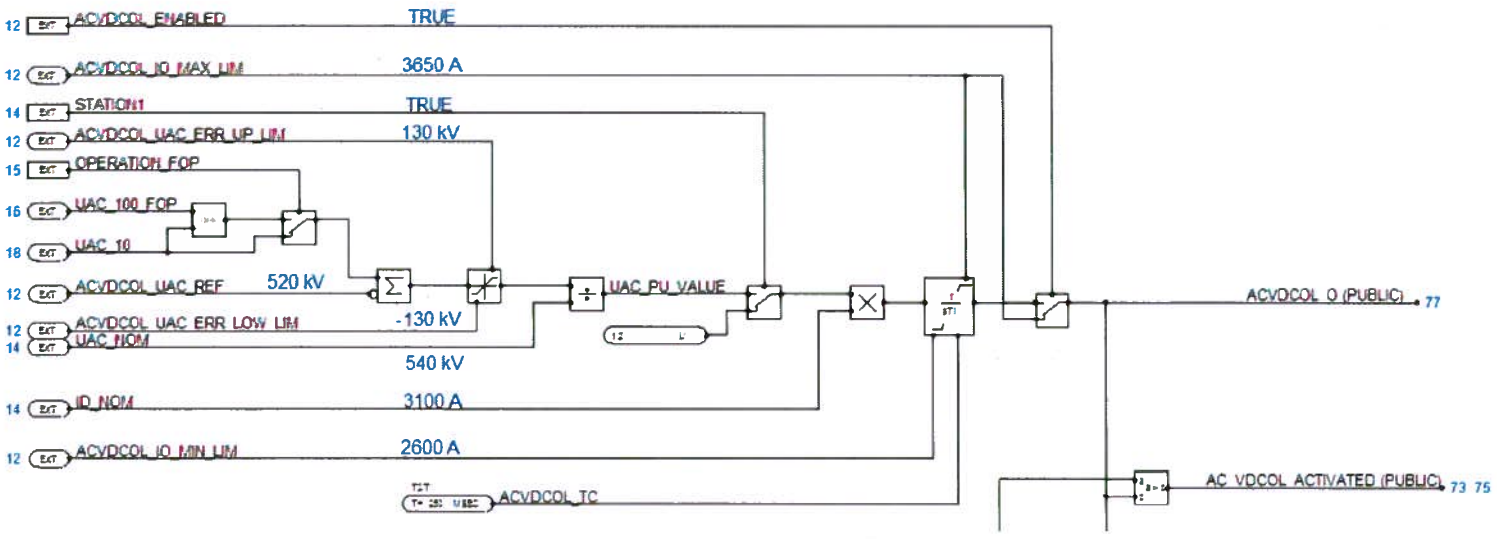
Reasons for suspending, modifying, or terminating the test sequence include but are not limited to the following:

- System emergency exists within the WECC
- Interconnections operating outside normal limits
- Undamped or unacceptable levels of system oscillations
- Facility operator deems that facility is unsafe for test, or that the test procedure is interfering with proper operation of that facility
- Test procedure is conflicting with a peak in operator workload
- A disturbance occurs resulting in system frequency below 59.85 Hz

If a disturbance occurs during a probing test, the test must be terminated immediately.

Additional Notification Procedure
If any AVR/PSS/PDCI Controller problems are observed notify the Transmission Operator immediately so that information can be communicated to the Generator Operator for their action.

AC-VDCOL Block-Diagram



6. Test Coordinator and Responsibilities

Test coordination will be as follows:

1. Test Director will schedule the tests through the BPA outage dispatcher.
2. Test Director (BPA technical staff) will post proposed test dates on the BPA Web page.
3. The day before each test, BPA will send a message on the WECC Net notifying of the tests.
4. If there are concerns about abnormal system conditions, BPA dispatcher should be contacted as early as possible to cancel a test. The test will be resumed the next hour after the system returns to normal.
5. The probing signal will be injected by an operator of Celilo converter station. The operator will clear with the BPA dispatcher before the signal injection.

A listing of contact persons and test observers with phone numbers and e-mail addresses will be provided 10 days in advance of the test.

A phone bridge will be available on the day of the test:

5. Sequence of Test Events

Test Series:

Test 1

1. Disable AC-VDCOL by setting ACVDCOL_ENABLED to FALSE
2. Verify PDCI power is at 3,000 MW or above.
3. Measure actual AC converter voltage
4. Set AC-VDCOL reference voltage 10-kV ABOVE the actual AC voltage by adjusting parameter ACVDCOL_UAC_REF
5. Enable AC-VDCOL by setting ACVDCOL_ENABLED to TRUE
6. Observe AC-VDCOL taking over the current order and ramping PDCI power down to 2,600 MW
7. Validate the AC-VDCOL integrator time constant using PMU recordings
8. Let the system settle
9. Disable AC-VDCOL by setting ACVDCOL_ENABLED to FALSE
10. Observe power return to 3,000 MW
11. Validate the AC-VDCOL integrator time constant
12. Set AC-VDCOL voltage reference parameter ADVDCOL_UAC_REF to 520 kV.
13. Enable AC-VDCOL by setting ADVDCOL_ENABLED to TRUE.

Test 2

1. Verify PDCI power is at 3,000 MW or above.
2. Disable AC-VDCOL by setting ACVDCOL_ENABLED to FALSE
3. **Operate Chief Joseph braking resistor**
4. Let the system oscillation settle
5. Enable AC-VDCOL by setting ADVDCOL_ENABLED to TRUE.

Test 3

1. Verify PDCI power is at 3,000 MW or above.
2. Disable AC-VDCOL by setting ACVDCOL_ENABLED to FALSE
3. Set AC-VDCOL voltage reference 3-kV BELOW the actual AC voltage by adjusting parameter ACVDCOL_UAC_REF
4. Enable AC-VDCOL by setting ACVDCOL_ENABLED to TRUE
5. **Operate Chief Joseph braking resistor**
6. Let the system oscillation settle
7. Observe AC-VDCOL operation during power swing
8. Disable AC-VDCOL by setting ACVDCOL_ENABLED to FALSE
9. Set AC-VDCOL voltage reference parameter ADVDCOL_UAC_REF to 520 kV.
10. Enable AC-VDCOL by setting ADVDCOL_ENABLED to TRUE.

As-left condition – return AC VDCOL settings to normal operation

1. Set AC-VDCOL voltage reference parameter ACVDCOL_UAC_REF to 520kV
2. Enable AC-VDCOL by setting ACVDCOL_ENABLED to TRUE

TEST APPROVALS

This test plan submitted by:

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